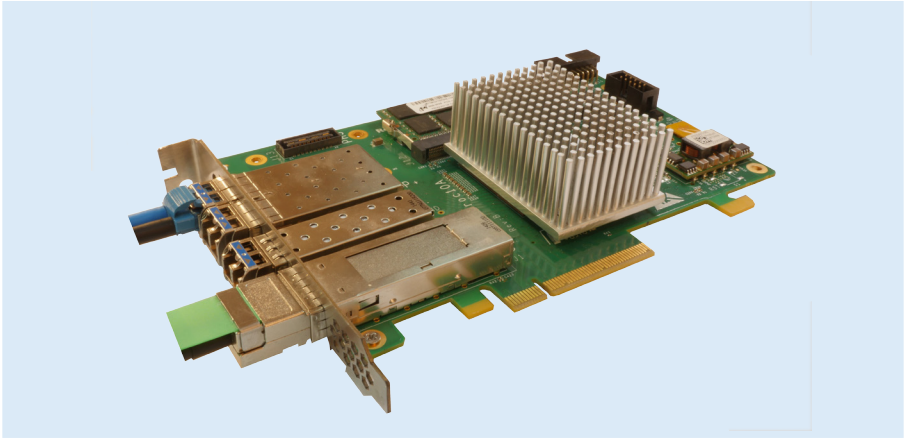
Proc10A

PCIe x8 (Gen. 3) FPGA Computation Accelerators

Key Features

- Altera Arria 10 FPGA (GX, SX), 1150
- PCIe x8 Gen. 3 or stand-alone
- Up to 15×14.2 Gb/s reconfigurable transceivers supporting multiple protocols and data rates
- Form factor: PCIe half-length
- Up to 40 GFLOPS-per-Watt
- 1x QSFP, 3x SFP+ and Gidel high-speed connectors
- Multi-level memory structure (32+ GB) Sustained throughput of 128+ TB/s for internal memories and ~16 GB/s for on-board memory as follows:
  - Enhanced MLAB (640-bit) SRAM blocks
  - Up to 2,713 M20K (20K-bit) SRAM blocks (53 Mb) at a typical throughput of 10 TB/s at 450 MHz
  - 1 GB DDR3 on-board memory at a maximum sustained throughput of 5.6 GB/s
  - 2x16 GB DDR4 ECC SoDIMM Banks for maximum sustained throughput of 19.2 GB/s
  - On board user flash (optional)
- Typical system freq: 150-450 MHz
- Flexible clocking system
- Low power (8-70W)
- Supported by Gidel's HLS (I++) ASP based on Intel's SDK
- Supported by Gidel's Proc Dev Kit:
  - Simultaneous acceleration of multiple applications or processes
  - Unmatched HDL design productivity
  - Simple integration with software applications



The Proc10A™ system is a flexible, high-performance, low-power FPGA platform based on Intel's powerful Arria 10 FPGA. The Proc10A's unique architecture balances high performance and flexibility to meet demanding and versatile compute acceleration requirements.

With up to fifteen 14.2 Gb/s full-duplex transceivers and vast memory resources, the Proc10A offers tremendous I/O throughput along with powerful on-board processing and data management capabilities ideal for low-latency, high-performance HPC, storage, networking, and high-end imaging applications. A multi-level memory scheme includes up to 32 GB DDR3 ECC SODIMM, 1 GB DDR3 SDRAM, dedicated FPGA memory blocks (M20K and MLABs), and other memory options.

In addition, the Proc10A hosts an 8-lane PCI Express Gen. 3 bridge that enables strong co-processing between the host CPU and the FPGA accelerator. For tightly-coupled FPGA and CPU processing, Gidel offers the Proc10A SoC family, with an embedded ARM processor based on the Arria 10 SoC FPGAs.

The Proc10A is supported by Gidel's High Level Synthesis (HLS) ASP and Gidel's innovative Proc Dev Kit enabling high productivity based on C and HDL designs. The kit generates the board ASP including the HDL interface envelop (PCIe, memory, etc.), user logic wrapper, board/IP constraints, and software and board drivers. The kit also includes an innovative memory controller enabling splitting the memory to independent logical units allowing simultaneous access of multiple applications.

Gidel
Committed to Your Innovation

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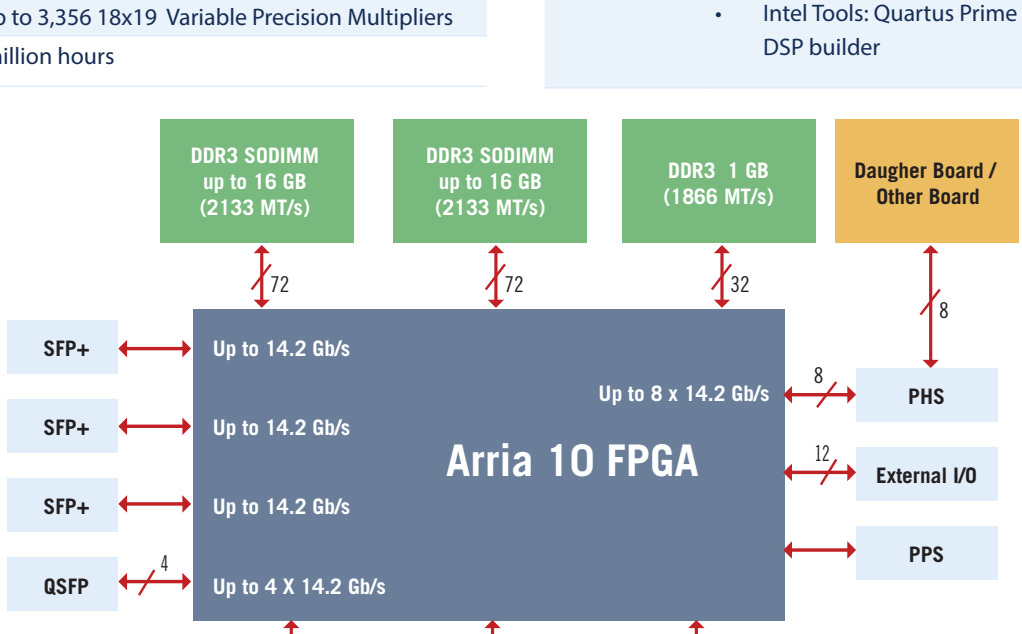
FEATURE	SPECIFICATIONS
FPGA	• Intel Arria 10 GX • Up to 1150K Logic Elements • Embedded 18x19 Multipliers • Embedded M20K and MLAB blocks • Up to 15x 12.5/14.1 Gb/s transceivers • 1.6 Gb/s LVDS performance
Memory	• Embedded MLAB (640-bit) SRAM blocks • M20K (20K-bit) SRAM blocks • Up to 32GB DDR4 SDRAM (2x SoDIMMs) • On board 2GB DDR4 SDRAM
Processing Performance	• Up to 2,713 M20K blocks @ 450 MT/s for total of ~10 TB/s • MLAB blocks@ 450 MT/s • Up to 1 GB DDR3 SDRAM for total of 5.6 GB/s • Up to 32 GB DDR3 SDRAM for a total of 19.2 GB/s • Up to 3,356 18x19 Variable Precision Multipliers
MTBF	> 1.5 million hours

FEATURE	SPECIFICATIONS
Host Interface	PCIe x8 Gen.3
I/O	1xQSFP, 3x SFP+ and Gidel PHS
GPIO	12x LVTTL
Board Management	• Flexible clocking system • Temperature monitoring • Internal Voltage monitoring

Development Tools	• HLS ASP for use with Intel's HLS compiler
	• Gidel ProDev Kit for HDL design flow:
	  • Generation of dedicated application driver.
	  • Splitting of physical on-board memories into logical memories with independent parallel access to/from user logic.
	  • Generation of environment FPGA code, including all board/IP constrains and user logic wrapper
	• Intel Tools: Quartus Prime Pro including QSys and DSP builder



Proc10A System Block Diagram

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